Claims:

1. (Previously Presented) An output-compensated buffer, comprising:

a buffer circuit that receives an input signal and produces an output signal responsive thereto at an output terminal, said buffer circuit including an input source-follower circuit that receives the input signal; and

a feedback circuit having an input connected to said output terminal and an output capacitively connected to a bias terminal of said input source follower circuit and operative to vary an input capacitance of said source follower circuit responsive to the output signal at said output terminal.

2.-3. (Canceled)

4. (Previously Presented) An output-compensated buffer according to Claim 1, wherein said feedback circuit is operative to variably capacitively couple the bias terminal to the power source responsive to the output signal at the output terminal.

5. (Original) An output-compensated buffer according to Claim 4, wherein said feedback circuit comprises a second source follower circuit having an input terminal that receives the output signal from the input source follower circuit of the buffer circuit and an output terminal capacitively coupled to the bias terminal of the input source follower circuit.

6. (Original) An output-compensated buffer according to Claim 5, wherein said second source follower circuit comprises:

a first transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit;

a second transistor having a drain terminal connected to the source terminal of the first transistor at a signal node, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

a capacitor coupled between the signal node and the bias terminal of the source follower circuit.

7. (Previously Presented) An output-compensated buffer according to Claim 1: wherein said source follower circuit comprises:

a first transistor having a source terminal, a gate terminal configured to receive the input signal, and a drain terminal connected to the power source through ~~the~~ a resistor; and

a second transistor having a drain terminal connected to the source terminal of the first transistor, a source terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

wherein said feedback circuit is coupled to the drain terminal of said first transistor.

8. (Original) An output-compensated buffer according to Claim 7, wherein said feedback circuit is capacitively coupled to the drain terminal of the first transistor.

9. (Original) An output-compensated buffer according to Claim 8, wherein said feedback circuit is operative to variably capacitively couple the drain terminal of the first transistor to the power source responsive to the output signal at the output terminal.

10. (Original) An output-compensated buffer according to Claim 9, wherein said feedback circuit comprises:

a third transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit;

a fourth transistor having a drain terminal connected to the source terminal of the third transistor, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

a capacitor coupled between the drain terminal of the fourth transistor and the drain terminal of the first transistor.

11. (Previously Presented) An output-compensated buffer according to Claim 1, wherein the output terminal of the buffer circuit is an output terminal of the source follower circuit.

12. (Previously Presented) An output-compensated buffer according to Claim 1, wherein the buffer circuit further comprises a second source follower circuit connected to an output of the input source follower circuit and operative to produce the output signal responsive to the input signal applied to the input source follower circuit.

13. (Original) An output-compensated buffer according to Claim 1, in combination with a CCD image capture device, wherein the CCD image capture device includes a horizontal transfer section that generates the input signal.

14. (Original) An output-compensated buffer, comprising:

a buffer circuit that receives an input signal and produces an output signal responsive thereto at an output terminal, said buffer circuit including an input source-follower circuit that has an input terminal that receives the input signal and a bias terminal that receives a bias voltage from a power source; and

a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and the bias terminal via a capacitor.

15. (Previously Presented) An output-compensated buffer according to Claim 14: wherein said source follower circuit comprises:

a first transistor having a source terminal, a gate terminal configured to receive the input signal, and a drain terminal connected to the power source through ~~the~~ a resistor; and

a second transistor having a drain terminal connected to the source terminal of the first transistor, a source terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

wherein said feedback circuit is coupled to the drain terminal of said first transistor.

16. (Original) An output-compensated buffer according to Claim 15, wherein said feedback circuit comprises:

a third transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit;

a fourth transistor having a drain terminal connected to the source terminal of the third transistor, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

a capacitor coupled between the drain terminal of the fourth transistor and the drain terminal of the first transistor.

17. (Original) An output-compensated buffer according to Claim 14, wherein the output terminal of the buffer circuit is an output terminal of the source follower circuit.

18. (Original) An output-compensated buffer according to Claim 13, wherein the buffer circuit further comprises a source follower circuit connected to an output of the input source follower circuit and operative to produce the output signal responsive to the input signal applied to the input source follower circuit.

19. (Original) An output-compensated buffer according to Claim 14 in combination with a CCD image capture device, wherein the CCD image capture device comprises a horizontal transfer section that generates input signal.

20. (Previously Presented) An image capture device, comprising:

a charged coupled device (CCD) that generates a video signal;

a buffer circuit responsive to the CCD and operative to receive the video signal and produce an output signal responsive thereto at an output terminal, said buffer circuit including an input source-follower circuit that receives the video signal; and

a feedback circuit having an input connected to said output terminal and an output capacitively coupled to a bias terminal of said input source follower circuit and operative to vary an input capacitance of said source follower circuit responsive to the output signal at said output terminal.

21. (Canceled)

22. (Original) An image capture device according to Claim 20, wherein said feedback circuit is operative to variably capacitively couple the bias terminal to the power source responsive to the output signal at the output terminal.